UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,284	10/05/2001	Kendell A. Chilton	EMC01-31(01129)	4870

7590 09/01/2005

David E. Huang, Esq.
CHAPIN & HUANG, L.L.C.
Westborough Office Park
1700 West Park Drive
Westborough, MA 01581

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,284	CHILTON, KENDELL A.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-14,16-21 and 23-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-14,16-21 and 23-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2-7, 9-14, 16-21, and 23-37 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE, Amendment, and Extension of Time as received on 6/23/2005.

Claim Objections

3. Claim 34 is objected to because of the following informalities: The use of the word "stores" in line 2 is improper because it is not clear how a circuit board stores a cache and a shared data structure. That is, how does hardware store hardware? Perhaps "stores" should be changed to "includes"? Appropriate correction is required.

4. Claim 35 is objected to because of the following informalities: The use of the word "stores" in line 3 is improper because it is not clear how a circuit board stores a cache and a shared data structure. That is, how does hardware store hardware? Perhaps "stores" should be changed to "includes"? Appropriate correction is required.

Withdrawn Rejections

5. Applicant, by way of amendment, has overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are hereby withdrawn by the examiner. However, upon further consideration, a new ground(s) of rejection is applied below.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 37 recites the limitation "the set of storage devices" in line 5.. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, this will be interpreted as "a set of storage devices".

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 2, 4-7, 9, 11-14, 16, 18-21, and 34-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Hotta et al., U.S. Patent No. 5,680,637 (herein referred to as Hotta).

11. Referring to claims 34-37, Hotta has taught in a data storage system having

(a) a set of storage devices. See Fig.2 and note the registers.

(b) a memory circuit board that stores:

(1) a cache to temporarily store copies of data elements stored in the set of storage devices. See Fig.13 and note the data cache. A data cache inherently stores data stored in registers due to the rules of memory hierarchy.

(2) a shared data structure utilized in managing the use of the cache. See Fig.1, and column 11, lines 40-44. Note that main memory is a shared data structure. Fig.13 shows that main memory is accessed through interface 1308 by at least the instruction cache controller and the data cache controller. Consequently, the main memory is a shared structure since it is shared by at least two components.

(c) a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices, the processor circuit board being operative with the memory circuit board to perform memory operations including:

(1) a basic operation to manipulate a memory location of the memory circuit board. See Fig.3 and note the load/store instruction, which read from/write to a memory location and read from/write to a register location.

(2) a complex operation to manipulate the shared data structure (Fig.3, compound instruction), a method by which the memory circuit board performs its part of the memory operations, comprising:

(i) receiving from the processor circuit board a communication that includes a command field and a payload field. See Fig.3 and note that the most significant bit (MSB) of the instruction is the command field (0 = basic, 1 = compound). Every other bit in the instruction makes up the payload.

(ii) determining whether the command field contains a basic write command or a script command, the basic write command being present when the communication is generated by the processor circuit board as part of the basic operation, the script command being present when the communication is generated as part of the complex operation. Again, if the command field = 0, then a basic read/write operation may be performed whereas if the command field = 1, then a complex operation is to be performed.

(iii) if the command field of the communication contains the basic write command, then writing data from the payload field of the communication into the memory location. See the store command (ST) of Fig.4 and note that the payload is used to locate data to be written to the memory location (which means it is also written to the data cache because caches hold the most recently accessed data).

(iv) if the command field of the communication contains the script command, then performing the following steps:

a) parsing the payload of the communication to identify a series of individual instructions. See the compound instruction of Fig.3 and note that it contains multiple instructions to be executed. Clearly, the payload must be parsed to determine what these instructions are.

b) performing a series of operations on the shared data structure according to the series of individual instructions. Note that each of the series of operations shown in the compound instruction of Fig.3 are performed on the shared structure (memory). For instance, a load/store operation are

performed on memory, and a prefetch may be performed from memory. See column 7, line 64, to column 8, line 3.

12. Referring to claim 2, Hotta has taught a method as described in claim 34. Hotta has further taught that the cache includes memory locations which store a data element (caches inherently have memory locations for storing data elements), wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element (for instance, load instruction), and wherein the step of performing the series of operations includes the steps of:

a) selecting the data element based on the address of the individual instruction. A load instruction inherently addresses the cache.

b) retrieving the data element from the memory locations of the cache. A load instruction inherently retrieves data from the cache.

c) performing an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation. And, the load operation inherently uses the retrieved data and stores it into a register within the processor.

13. Referring to claim 4, Hotta has taught a method as described in claim 34. Hotta has further taught that the steps of parsing and performing occur as an atomic operation. As is known with VLIW instructions, which Hotta's compound instruction is, each of the operations within a VLIW instruction are performed in parallel without being interrupted. Therefore, execution is atomic.

14. Referring to claim 5, Hotta has taught a method as described in claim 34. Hotta has further taught the steps of:

a) generating a series of results in response to performing the series of operations. Clearly, instructions that are performed will generate results.

b) providing the series of results to a processor circuit board. Clearly, instructions which are to update registers will provide results to the registers.

15. Referring to claim 6, Hotta has taught a method as described in claim 5. Hotta has further taught that the step of providing the series of results to the processor circuit board includes the steps of:

a) packaging the series of results in a set of data blocks. Since VLIW operations are performed in parallel, results will be generated in parallel. The results make up data blocks.

b) transferring the set of data blocks to the processor circuit board. The data blocks are then transferred to registers, for instance.

16. Referring to claim 7, Hotta has taught a method as described in claim 34. Hotta has further taught loading a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations. Note from Figs.3-4 that load instructions exist within Hotta's system. As is known, load instructions load registers with data (constants) which are used as operands (parameters) in later instructions such as Add instructions. Or an Add instruction may produce a result which is stored in a register that is later to be stored into main memory in response to a store instruction.

17. Referring to claim 9, Hotta has taught a system as described in claim 35. The system of claim 9 performs the method of claim 2. Consequently, claim 9 is rejected for the same reasons set forth in the rejection of claim 2.

18. Referring to claim 11, Hotta has taught a system as described in claim 35. The system of claim 11 performs the method of claim 4. Consequently, claim 11 is rejected for the same reasons set forth in the rejection of claim 4.

19. Referring to claim 12, Hotta has taught a system as described in claim 35. The system of claim 12 performs the method of claim 5. Consequently, claim 12 is rejected for the same reasons set forth in the rejection of claim 5.

20. Referring to claim 13, Hotta has taught a system as described in claim 12. The system of claim 13 performs the method of claim 6. Consequently, claim 13 is rejected for the same reasons set forth in the rejection of claim 6.

21. Referring to claim 14, Hotta has taught a system as described in claim 35. The system of claim 14 performs the method of claim 7. Consequently, claim 14 is rejected for the same reasons set forth in the rejection of claim 7.

22. Referring to claim 16, Hotta has taught a board as described in claim 36. The board of claim 16 performs the method of claim 2. Consequently, claim 16 is rejected for the same reasons set forth in the rejection of claim 2.

23. Referring to claim 18, Hotta has taught a board as described in claim 36. The board of claim 18 performs the method of claim 4. Consequently, claim 18 is rejected for the same reasons set forth in the rejection of claim 4.

24. Referring to claim 19, Hotta has taught a board as described in claim 36. The board of claim 19 performs the method of claim 5. Consequently, claim 19 is rejected for the same reasons set forth in the rejection of claim 5.

25. Referring to claim 20, Hotta has taught a board as described in claim 19. The board of claim 20 performs the method of claim 6. Consequently, claim 20 is rejected for the same reasons set forth in the rejection of claim 6.

26. Referring to claim 21, Hotta has taught a board as described in claim 36. The board of claim 21 performs the method of claim 7. Consequently, claim 21 is rejected for the same reasons set forth in the rejection of claim 7.

27. Claims 3, 10, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta, as applied above, in view of Narayan et al., U.S. Patent No. 5,748,978 (as applied in the previous Office Action and herein referred to as Narayan).

28. Referring to claim 3, Hotta has taught a method as described in claim 34. Hotta has not taught that the memory circuit board further stores an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the step of performing the series of operations includes the steps of:

a) referencing the section of the code of the instruction library based on the instruction reference.

b) executing the section of code.

However, Narayan has taught the implementation of an MROM unit, which as discussed in column 8, lines 10-19, is used to break down complex instructions into smaller, less complicated routines, which are then executed to perform the operation specified by the complex instruction. Clearly, if an instruction is broken down into a set of smaller instructions, then the instruction will determine which set of instructions are executed. As discussed, an MROM is

hardware used to efficiently decode complex instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hotta to include an MROM unit.

29. Referring to claim 10, Hotta has taught a system as described in claim 35. The system of claim 10 performs the method of claim 3. Consequently, claim 10 is rejected for the same reasons set forth in the rejection of claim 3.

30. Referring to claim 17, Hotta has taught a board as described in claim 36. The board of claim 17 performs the method of claim 3. Consequently, claim 17 is rejected for the same reasons set forth in the rejection of claim 3.

31. Claims 23-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta, as applied above.

32. Referring to claim 23, Hotta has taught a method as described in claim 34.

a) Hotta has further taught that the series of individual instructions of the payload has a positional order and processing the series of individual instructions in the positional order within the memory circuit board. See Fig.3, and note that each of the operations within the compound instruction (VLIW instruction) have a corresponding position.

b) Hotta has further taught that the processing within the memory circuit board effectuates temporary caching of data within the memory circuit board. When a store operation is performed, the data is written to the data cache as it's the most recently accessed item, and the duty of the cache is to store recently accessed items. Hotta has not explicitly taught that the data is en route between an external host and a set of disk drives of the data storage system.

However, disks are well known and accepted in the art. A disk allows for mass storage at a relatively cheap price. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hotta to include a disk coupled to the processor. Furthermore, as is known with a memory hierarchy, data always ultimately travels to the highest level. That is, if data is to be stored from a register, it will be stored in the cache, main memory, and ultimately disk.

33. Referring to claim 24, Hotta has taught a method as described in claim 23. Hotta has not explicitly taught that the step of receiving the communication includes the step of acquiring the communication including the script command and the payload, which has the series of individual instructions, from a processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload. However, recall that it would have been obvious to have multiple memories in a hierarchy (such as disk drives). A system may have registers, cache, main memory, disk drives, etc. This allows the system to store massive amounts of data while also allowing for fast retrieval of most data. As a result, in order to achieve such a hierarchy, it would have been obvious to one of ordinary skill in the art at the time of the invention to have multiple memory circuit boards (multiple caches/memories/disks). Consequently, there must be a bus connecting each memory board to the processor board (multi-drop bus) for allowing operations to be performed on the respective memories.

34. Referring to claim 25, Hotta has taught a system as described in claim 35. Furthermore, the system of claim 25 performs the method of claim 23. Consequently, claim 25 is rejected for the same reasons set forth in the rejection of claim 23.

35. Referring to claim 26, Hotta has taught a system as described in claim 25. Furthermore, the system of claim 26 performs the method of claim 24. Consequently, claim 26 is rejected for the same reasons set forth in the rejection of claim 24.

36. Referring to claim 27, Hotta has taught a board as described in claim 36. Furthermore, the board of claim 27 performs the method of claim 23. Consequently, claim 27 is rejected for the same reasons set forth in the rejection of claim 23.

37. Referring to claim 28, Hotta has taught a board as described in claim 27. Furthermore, the board of claim 28 performs the method of claim 24. Consequently, claim 28 is rejected for the same reasons set forth in the rejection of claim 24.

38. Referring to claim 29, Hotta has taught a board as described in claim 37. Furthermore, the board of claim 29 performs the method of claim 23. Consequently, claim 29 is rejected for the same reasons set forth in the rejection of claim 23.

39. Referring to claim 30, Hotta has taught a board as described in claim 29. Furthermore, the board of claim 30 performs the method of claim 24. Consequently, claim 30 is rejected for the same reasons set forth in the rejection of claim 24.

40. Referring to claim 31, Hotta has taught a method as described in claim 24. Hotta has further taught that the step of processing the series of individual instructions in the positional order within the memory circuit board includes the step of completely carrying out a complex task in an atomic manner, the complex task resulting from execution of each individual

instruction of the series of individual instructions in the positional order. As shown in Fig.3, the compound instruction (VLIW instruction) contains a series of operations in an order. This order of operations is carried out atomically (in parallel) as is known in VLIW systems.

41. Referring to claim 32, Hotta has taught a system as described in claim 26. Furthermore, claim 32 is rejected for the same reasons set forth in the rejection of claim 31.

42. Referring to claim 33, Hotta has taught a board as described in claim 28. Furthermore, claim 33 is rejected for the same reasons set forth in the rejection of claim 31.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
August 18, 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100